WHAT IS CLAIMED IS:

1. A memory cell comprising:

a storage electrode for storing charge, wherein the storage electrode includes a material selected from the group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN); and

an insulator adjacent to the storage electrode.

2. The memory cell of claim 1, wherein materials comprising at least one of the storage electrode and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

3. The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired data charge retention time of less than or equal to approximately 40 seconds at 250 degrees Celsius.

4. The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired erase time of less than approximately 1 second.

5. The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired erase voltage of less than approximately 12 Volts.

6. The memory cell of claim 1, wherein the insulator comprises a material that has a larger electron affinity than silicon dioxide.

7. The memory cell of claim 1, wherein a material composition of the storage electrode is selected to obtain a smaller electron affinity than polycrystalline silicon.

8. The memory cell of claim 1, wherein the barrier energy is less than approximately 2.0 eV.

9. The memory cell of claim 1, wherein the storage electrode is isolated from conductors and semiconductors.

10. The memory cell of claim 1, wherein the storage electrode is transconductively capacitively coupled to a channel

11. A transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, wherein the floating gate includes a material selected from the group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN).

12. The transistor of claim 11, wherein materials comprising at least one of the storage electrode and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

13. The transistor of claim 12, wherein the barrier energy provides a data charge retention time of the transistor that is adapted for dynamic refreshing of charge stored on the floating gate.

14. The transistor of claim 11, wherein the floating gate is isolated from conductors and semiconductors.

15. The transistor of claim 11, wherein the insulator comprises a material that has a larger electron affinity than silicon dioxide.

16. The transistor of claim 11, wherein the floating gate includes a material composition of the storage electrode is selected to obtain a smaller electron affinity than polycrystalline silicon.

17. The transistor of claim 11, further comprising a control electrode, separated from the floating gate by an intergate dielectric.

18. The transistor of claim 17, wherein the area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than the area of a capacitor formed by the floating gate, the insulator, and the channel region

19. The transistor of claim 17, wherein the intergate insulator has a permittivity that is higher than a permittivity of silicon dioxide.

20. The transistor of claim 11, wherein the floating gate is capacitively separated from the channel region for providing transconductance gain.

21. A method of using a floating gate transistor having a floating gate electrode that includes a material selected from the group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN), the method comprising:

storing data by changing the charge of the floating gate;

reading data by detecting a current between a source and a drain; and

refreshing data based on a data charge retention time that depends upon a barrier energy at an interface between an insulator and the floating gate electrode.

22. The method of claim 21, wherein storing data by changing the charge of the floating gate transconductively provides an amplified signal between the source and the drain.

23. The method of claim 21, wherein the detected current is based on the charge of the floating gate and a transconductance gain of the floating gate transistor.

24. A method of forming a floating gate transistor, the method comprising:

forming source and drain regions;

forming a gate insulator from the gate insulator material; and

forming a floating gate from a floating gate material selected from the group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN), such that the floating gate is isolated from conductors and semiconductors.

25. The method of claim 24, wherein forming the floating gate includes depositing the floating gate material by metal organic chemical vapor deposition (MOCVD).

26. The method of claim 24, wherein forming the floating gate includes forming the floating gate material by plasma-enhanced molecular beam epitaxy (PEMBE).

27. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, wherein the floating gate includes a floating gate material selected from the

group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN); and

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric.

28. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, wherein the floating gate includes a floating gate material selected from the group consisting essentially of gallium nitride (GaN) and gallium aluminum nitride (GaAlN); and

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric; and

the memory device further comprising a refresh circuit dynamically refreshing, at a refresh rate, data stored on the floating gates of the transistors.

29. The memory device of claim 28, wherein the refresh rate is based on a barrier energy between the floating gate and the insulator.